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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Rajendra K. Taluri et al.
Serial No:	09/632,543
Filed:	8/4/2000
Art Unit:	2612
Examiner:	L. Nguyen
Docket No.:	TI-28919
Conf. No.:	1760
Customer No.:	23494

CERTIFICATION OF FACSIMILE TRANSMISSION

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Gracia Sansom — 5-2-05

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FACSIMILE COVER SHEET

X FACSIMILE COVER SHEET (1 SHEET)	___ AMENDMENT
___ NEW APPLICATION	___ EOT
___ DECLARATION	___ NOTICE OF APPEAL
___ ASSIGNMENT	X APPEAL BRIEF (5 Pages)
___ FORMAL DRAWINGS	___ ISSUE FEE
___ INFORMAL DRAWINGS	___ REPLY BRIEF (IN TRIPLICATE)
___ CONTINUATION APP'N	___
___ DIVISIONAL APP'N	

NAME OF INVENTOR(S): Rajendra K. Taluri et al.	RECEIPT DATE & SERIAL NO.: **Serial No.: 09/632,543**
TITLE OF INVENTION: Digital Still Camera System and Method	**Filing Date: 8/4/2000**
TI FILE NO.: **TI-28919** / DEPOSIT ACCT. NO.: **20-0668**	**Conf. No.: 1760**
FAXED: **05/02/2005**	
DUE: **05/01/2005**	
ATTY/SECY: **CHH/gs**	

Texas Instruments Incorporated
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Dallas, TX 75265

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl.No.:	09/632,543	Confirmation No.: 1760
Appellant:	Talluri et al	
Filed:	August 4, 2000	
TC/AU:	2612	
Examiner:	Nguyen	
Docket:	TI-28919	
Cust.No.:	23494	

APPELLANTS' BRIEF

Commissioner for Patents
P.O.Box 1450
Alexandria VA 22313-1450

Sir:

The attached sheets contain the Rule 41.37 items of appellants' brief. The Commissioner is hereby authorized to charge the fee for filing a brief in support of the appeal plus any other necessary fees to the deposit account of Texas Instruments Incorporated, account No. 20-0668. A fee transmittal sheet is enclosed.

Respectfully submitted,

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Rule 41.37(c)(1)(i) Real party of interest

Texas Instruments Incorporated owns the application.

Rule 41.37(c)(1)(ii) Related appeals and interferences

There are no related dispositive appeals or interferences.

Rule 41.37(c)(1)(iii) Status of claims

Claims 1 and 3-6 are pending in the application with all claims finally rejected. This appeal involves the finally rejected claims.

Rule 41.37(c)(1)(iv) Status of amendments

There is no amendment after final rejection.

Rule 41.37(c)(1)(v) Summary of claimed subject matter

The invention provides an integrated circuit for a digital camera which includes at least processors, a first programmable processor related to a user interface and control, a second programmable processor for image processing and compression, and a third processor for other operations. Application Figure 1b illustrates a preferred embodiment with a first processor 130 (ARM), a second processor 122 (DSP), and various third processors: 124 (imaging extension), 108 (burst mode compression/decompression), and 126 (VLC). Application pages 4-6 provide a terse summary of various operations of the processors.

Rule 41.37(c)(1)(vi) Grounds of rejection to be reviewed on appeal

The grounds of rejection to be reviewed on appeal are:

(1) whether claims 1, 3, and 6 are patentable over the Safai reference in view of the Mizutani reference.

(2) whether claim 4 is patentable over the Safai reference in view of the Fukuoka reference.

(3) whether claim 5 is patentable over the Safai reference in view of the Mizutani and Fukuoka references.

Rule 41.37(c)(1)(vii) Arguments

(1) Claims 1, 3, and 6 were rejected as unpatentable over Safai in view of Mizutani.

With regard to claim 1, the Examiner cited Safai processors 312 and 310 of Fig.3 for the first and second processors of the claim and cited Mizutani Fig. 7 multipliers 85-87, 95-97 and adders 88-90, 98-100 for the multiply and accumulate units of the claim.

Appellants reply that the cited multipliers and adders of Mizutani do not form multiply and accumulate units because there is no accumulation. The accumulate function is an addition to the current contents to yield updated contents; see application Fig.19. In contrast, the adders of Mizutani have two inputs with neither being a feedback of the current contents; indeed, the adders of Mizutani do not retain outputs as required for accumulators.

With regard to claim 3, the Examiner applied Safai as before cited Mizutani JPEG unit 29 as the image compression unit.

Appellants reply that claim 3 requires the image compression unit be able to act on the acquired image; in contrast, Mizutani Fig.2 shows JPEG unit 29 applies after input processing 21 and thus not acting on the acquired image. Application Fig.1b shows burst mode compression/decompression unit 108 directly connected to the CCD controller to get the acquired image.

With regard to claim 6, the Examiner applied Safai as before cited Mizutani for camera peripherals.

Appellants rely upon the patentability of parent claim 1.

(2) Claim 4 was rejected as unpatentable over Safai in view of Fukuoka; the Examiner cited Fukuoka processing circuit 4 in addition to Safai as before.

Appellants reply that claim 4 requires a digital image processing unit, whereas Fukuoka processing circuit 4 is analog.

(3) Claim 5 was rejected as unpatentable over Safai in view of Mizutani and Fukuoka. The Examiner cited Fukuoka for audio input.

Appellants rely upon the patentability of parent claim 1.

Rule 41.37(c)(1)(viii) Claims appendix

1. An integrated circuit for a digital still camera, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) a third processor coupled to said second processor, said third processor including at least four parallel multiply and accumulate units.

3. An integrated circuit for a digital still camera, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) an image compression unit separate from said second processor, said compression unit arranged to compress acquired images for storage in a memory and to decompress said compressed acquired images in said memory for restorage in said memory.

4. An integrated circuit for a digital still camera, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) a digital image processing unit separate from said first and second processors, said image processing unit arranged for real-time image sequence (video) processing, said image processing unit controlled in real-time by said first processor

5. The integrated circuit of claim 1, further comprising:

(a) an audio input coupled to said second processor, said second processor programmed to decode audio and said first processor programmed to output said decoded audio.

6. The integrated circuit of claim 1, further comprising:

(a) camera peripherals including IfSA, USB, NTSC/PAL encoder, and compact flash/smart media interface.

Rule 41.37(c)(1)(ix) Evidence appendix

n/a

Rule 41.37(c)(1)(x) Related proceedings appendix

n/a